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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,188	01/31/2001	Truc Duy Nguyen	AUS920000757US1	4492
7590 12/03/2003			EXAMINER	
Duke W. Yee Carstens, Yee & Cahoon, LLP P.O. Box 802334			NGUYEN, HAU H	
			ART UNIT	PAPER NUMBER
Dallas, TX 75380			2676	
			DATE MAILED: 12/03/2003	\rightleftharpoons

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
	09/773,188	NGUYEN ET AL.				
Office Action Summary	Examiner	Art Unit				
	Hau H Nguyen	2676				
The MAILING DATE of this communi Period for Reply	ication appears on the cover sheet w	ith the correspondence address				
A SHORTENED STATUTORY PERIOD FOTHE MAILING DATE OF THIS COMMUNII - Extensions of time may be available under the provisions after SIX (6) MONTHS from the mailing date of this community of the period for reply specified above is less than thirty (30). - If NO period for reply is specified above, the maximum states of the period for reply is specified above, the maximum states of the period for reply. - Any reply received by the Office later than three months at earned patent term adjustment. See 37 CFR 1.704(b). Status	CATION. of 37 CFR 1.136(a). In no event, however, may a r unication. D) days, a reply within the statutory minimum of thir atutory period will apply and will expire SIX (6) MON will, by statute, cause the application to become AE	reply be timely filed ty (30) days will be considered timely. ITHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).				
1)⊠ Responsive to communication(s) file	d on 22 September 2003.					
<u> </u>	b)⊠ This action is non-final.					
3) Since this application is in condition	 Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. 					
Disposition of Claims						
4) ☐ Claim(s) <u>1-30</u> is/are pending in the a 4a) Of the above claim(s) <u>19</u> is/are w 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) <u>1-18, 20-30</u> is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restrice	ithdrawn from consideration.					
8) Claim(s) are subject to restricApplication Papers	don and/or election requirement.					
· · ·	- Evaminar					
9) The specification is objected to by the 10) The drawing(s) filed on is/are: Applicant may not request that any object Replacement drawing sheet(s) including 11) The oath or declaration is objected to	a) accepted or b) objected to ction to the drawing(s) be held in abeyar the correction is required if the drawing	nce. See 37 CFR 1.85(a). (s) is objected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. §§ 119 and 120						
· · · · · · · · · · · · · · · · · · ·	documents have been received. documents have been received in A of the priority documents have been nal Bureau (PCT Rule 17.2(a)). In for a list of the certified copies not or domestic priority under 35 U.S.C. d in the first sentence of the specific guage provisional application has b or domestic priority under 35 U.S.C.	received in this National Stage received. § 119(e) (to a provisional application) ation or in an Application Data Sheet. een received. §§ 120 and/or 121 since a specific				
Attachment(s)						
1) ☑ Notice of References Cited (PTO-892) 2) ☑ Notice of Draftsperson's Patent Drawing Review (P' 3) ☑ Information Disclosure Statement(s) (PTO-1449) Pa	TO-948) 5) Notice of I	Summary (PTO-413) Paper No(s) nformal Patent Application (PTO-152)				

Response to Arguments

1. Applicant's arguments filed September 22, 2003, with respect to the rejection(s) of claims 1-30 under have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Peddada et al. (US 6,295,068).

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1-18, 20-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders (U.S. Patent No. 5,917,497) in view of Peddada et al. (U.S. Patent No. 6,295,068).

Referring to claims 1, 8-9, 11-13, 15, 20, 27-28, and 30, Saunders teaches an algorithm is provided which is able to compute the total memory needed to store a full MIP map based on the first level that is passed to the graphics core as well as on subsequent base map level changes. Each level is then stored into the contiguous memory, if the level is valid, or in a temporary memory location, if the level is not valid. Each time the base level changes, all levels are tested for validity, and the valid levels, are placed into the contiguous memory (col. 4, lines 21-29). Saunders further teach it is first determined whether sufficient memory exists to place all of the texel data into a single block of memory. With reference to FIG. 2, this determination is illustrated by decision block 14. If it is not known whether there is sufficient memory, then we must compute the size of the contiguous memory block which will be needed 16, and the memory must be allocated 18 (col. 4, lines 60-66). If it is determined that sufficient memory

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could not be allocated 20, an error condition 22 will result. Alternatively, the base map (Level 0) values will be stored 24, and then a check is made to determine if the Level information is OK 28. By this, what is meant is that a determination is made as to whether or not the information associated with the MIP map level being loaded is consistent with the information previously known about the MIP map (col. 5, lines 13-22) (halting step in response to absence of stored texture object). Allocating memory for the next level and freeing of memory is illustrated in Fig. 4 (step 96) and Fig. 5 (steps 19, 29).

Thus, Saunders teach all the limitations of claims 1, 11-13, 15, 20, and 30, except that in response to the halting step, the method allocating memory in the second memory by selectively removing stored texture.

However, Peddada et al. teach a method for managing texture, wherein as shown in Fig. 6, when the texture is not yet in the texture cache, handle AGP texture process 74 calls cache space process 95. Cache space process 95 calls best-fit process 96, which examines the free addresses and the required size for the new texture block, and chooses one block in the texture cache to put the new texture. The address of the selected block is returned to cache space process 95. Handle AGP texture process 74 maintains a lookup table of the texture blocks in the texture cache. When best-fit process 96 is unable to locate a free block that is large enough to contain the new texture, cache space process 95 calls free-block process 98. Free-block process 98 finds the least-recently-used (LRU) texture in the cache and invalidates it (selectively removing texture). The address of the invalidated texture block is returned. The size of the new texture can be sent to free-block process 98 so that the least-recently-used texture that has a size at least as large as the needed size can be chosen rather than simply the LRU block. Once a sufficiently

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large block in the texture cache has been found by cache space process 95, handle AGP texture process 74 activates the DMA transfer engine by calling AGP DMA process 88. AGP DMA process 88 performs the copy of the texture from the AGP portion of the main memory to the texture cache in the graphics memory. The address for the new texture block found by cache space process 95 is used by the DMA as the destination address (col. 7, lines 35-67). As shown in Fig. 5, Peddada et al. teach a bus system, memory connected to the bus system, and a CPU connected to the bus system.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Saunders in combination with the method as taught by Peddada et al. in order to simplify interface between the high-level application program and the graphics driver (col. 3, lines 51-58).

In regard to claims 2-5, 21-24, although Saunders does not teach the first memory is a system memory or an advanced graphic port memory, and the second memory is a frame buffer or a kernel application, Peddada et al. teach the first memory is the main memory 12 or AGP 14, and the second memory is the frame buffer 22, or the texture cache 24 as shown in Fig. 5.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Saunders in combination with the method as taught by Peddada et al. in order to simplify interface between the high-level application program and the graphics driver (col. 3, lines 51-58).

Referring to claims 6 and 25, as cited above, Saunders teaches assigning the first memory to an application (client application).

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In regard to claims 7, 10, 26, and 29, although Saunders does not teach the stored texture object is texture object used less than a threshold value, as cited above, Peddada et al. teach Free-block process 98 finds the least-recently-used (LRU) texture (used less than a threshold value) in the cache and invalidates it. The address of the invalidated texture block (an identifier) is returned.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Saunders in combination with the method as taught by Peddada et al. in order to simplify interface between the high-level application program and the graphics driver (col. 3, lines 51-58).

In regard to claim 14, although Saunders does not teach the memory management system having a first texture manager and a second texture manager, as shown in Fig. 5 and as cited above, it can be implied from Peddada et al. reference that the AGP memory and the texture cache each has its own texture manager for managing in and out texture.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Saunders in combination with the method as taught by Peddada et al. in order to simplify interface between the high-level application program and the graphics driver (col. 3, lines 51-58).

Referring to claims 16-18, although Saunders does not teach a bus system and a processor unit, Peddada et al. a system bus with plurality of buses, and the processor unit can comprise plurality of processors.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Saunders in combination with the method as taught by Peddada et al. in order to

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simplify interface between the high-level application program and the graphics driver (col. 3, lines 51-58).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

11/25/2003

MATTHEW C. BELLA SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2600

Marker (Bella